

OCT 06 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:
Deshpande et al.

Serial No.: 10/709,048

Filed: April 8, 2004

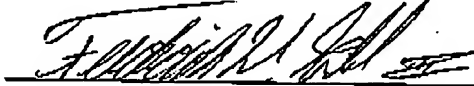
Group Art Unit: 2814

Examiner: Ingham, John C.

Atty. Docket No.: FIS920030397US1

Certificate of Transmission by Facsimile

I hereby certify that this correspondence is
being facsimile transmitted to the United
States Patent and Trademark Office (Fax No.
571-273-8300) on 10-0-05


Frederick W. Gibb, III

For: A MANUFACTURABLE METHOD AND STRUCTURE FOR DOUBLE SPACER
CMOS WITH OPTIMIZED NFET/PFET PERFORMANCE

Commissioner of Patents
PO BOX 1450
Alexandria, VA 22313-1450

RESPONSE TO RESTRICTION REQUIREMENT

Sir:

In response to the Office Action dated September 30, 2005, please consider the following:

10/709,048

1